



UNITED STATES PATENT AND TRADEMARK OFFICE

mm
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|-----------------------|------------------|
| 10/768,108 | 02/02/2004 | Jamal Ramdani | 248397US99DIV | 5746 |
| 22850 | 7590 | 06/23/2004 | EXAMINER | |
| OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314 | | | BAUMEISTER, BRADLEY W | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2815 | |

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

4/1

| | | | |
|------------------------------|--|---------------------------------------|--|
| Office Action Summary | Application No. 10/768,108 | Applicant(s) RAMDANI ET AL. | |
| | Examiner B. William Baumeister | Art Unit 2815 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 144-163 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 144-163 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 144-163 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guenzer '653 in view of JP 52-89070 and Kaushik et al., "Device Characteristics of Crystalline Epitaxial Oxides on Silicon;" Device Research Conference, 2000, Conference Digest 58th DRC, pp. 17-20, June 19-21, 2000.

- a. Guenzer '653 teaches a semiconductor layer 14 which may either be composed of Si or a compound semiconductor (see e.g., col. 3, lines 55-) and that is formed over a monocrystalline Si substrate 22 by means of a perovskite layer such as bismuth titanate (BiTO) 12 or others (col. 3, lines 45-55) and an amorphous SiO_x layer 24. Guenzer does not read on those limitations of the claims that set further forth that the perovskite layer and the overlying compound semiconductor layer are monocrystalline. Rather, Guenzer teaches that the epitaxial perovskite is "crystallographically oriented" which he defines to mean strongly oriented in the c-axis direction, but that the a- and b- axis directions possess a mosaic crystalline structure (e.g., col. 2, lines 5-44). Guenzer further states that the crystallographically oriented perovskite causes the resultant superposed epitaxial layer to also be a crystallographically oriented layer that does not have the higher quality

of singly crystalline semiconductor material, but which is better than polycrystalline layers, so that transistors should be able to be formed therein (col. 4, lines 12-20).

- i. To summarize, Guenzer teaches that the long-sought industry goal of monolithically integrating compound semiconductor layers with devices formed therein on monocrystalline Si substrates can be achieved by means of perovskite buffers. It teaches that crystalline imperfections in the perovskite buffer will produce crystalline imperfections in this overlying epitaxial device layer. And Guenzer provides motivation as to why one would have desired to further improve upon this invention so as to form a monocrystalline buffer and therefor a monocrystalline epitaxial device layer instead of ones that are crystallographically oriented: to produce higher quality transistors or devices.
- b. JP '070 teaches the growth of monocrystalline (100) Si, III-Vs (such as GaAs, GaP and InP) or II-VIs (such as ZnSe and ZnTe) on monocrystalline (001) or (100) perovskite oxides such as strontium titanate (STO) and barium titanate (BTO). Restated, JP '070 provides further evidence that it was known to those skilled in the art that if a perovskite layer were monocrystalline instead of crystallographically oriented, the compound semiconductor layer(s) formed on the perovskite could also be formed to have the preferable monocrystalline structure instead of a crystallographically-oriented structure. Thus, the primary remaining issue is whether it was known how to form perovskites on a monocrystalline silicon substrate so as to enable the perovskite to also be monocrystalline.

Art Unit: 2815

c. Kaushik teaches the growth of monocrystalline epitaxial perovskite oxides such as STO over monocrystalline substrates which produces an amorphous SiO_x interface layer therebetween. The STO unit cell is rotated 45° relative to the Si unit cell (e.g., Introduction, pg. 17). The STO perovskite can be formed to have a thickness on the order of 10 nm (e.g., Device Fabrication, page 17), and the thickness of the amorphous SiO_x interface is about 1 nm (Physical Characterization of the Film, page 18). The article does not teach the further inclusion of a compound semiconductor layer on top of the monocrystalline perovskite oxide.

d. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed compound semiconductor device layers so as to be monolithically integrated on monocrystalline Si substrates by means of a perovskite buffer layer as taught by Guenzer. It would have further been obvious to one of ordinary skill in the art at the time of the invention that both the perovskite and compound semiconductor layers formed on the monocrystalline Si substrate could be formed so as to also be monocrystalline instead of merely being crystallographically oriented (which Guenzer teaches is desirable for forming better quality devices or components therein) by employing particular perovskites such as at least STO with an amorphous SiO_x substrate/perovskite interface layer as taught by the combined teachings of Kaushik and JP '070.

e. Further, it was well known to those of ordinary skill in the art at the time of the invention to form a wide array of active and passive devices on compound semiconductor layers instead of Si for various reasons such as (1) for producing devices and circuits that

have higher frequencies and/or faster operation than is afforded by Si; and (2) because unlike Si, many conventional compound semiconductors are direct bandgap materials, enabling the formation of optoelectronic devices such as light emitters, detectors and modulators. Such conventional compound semiconductors include many of the III-Vs (e.g, III-As, III-P, III-N and combinations thereof) and the II-VIs.

f. Moreover, it has been a decades-long-sought industry goal to be able to reliably form compound semiconductor layers on Si substrates (1) for the purpose of integrating compound semiconductor devices with Si devices on a single chip because this would reduce the number, size and/or total space of required components and reduce the length or eliminate the number of requisite, associated electrical interconnections; and (2) because the elimination of the need for a compound semiconductor wafer would greatly reduce the manufacturing costs since Si substrates are so much cheaper to produce than compound semiconductor wafers. While this desire to form compound semiconductor layers on Si substrates was conventional, the ability to actually do so has generally proven difficult because of the dissimilarities that exist between various properties of Si and the compound semiconductors, such as their dissimilar lattice constants.

Conventional attempts to form compound semiconductors on Si have previously included schemes such as the use of wafer-bonding techniques and the use of intermediate buffer layers.

g. Since the prior art teaches that it was obvious at the time of the invention to have formed the compound semiconductor layer on the substrate by means of the specific buffer layer(s) as presently claimed, it would have further been obvious to one of

Art Unit: 2815

ordinary skill in the art at the time of the invention to have formed the specifically recited components on the compound semiconductor layer and the Si layer, since the particular devices/circuits were conventional, there was a strong and widely known motivation in the industry to integrate compound and Si semiconductor devices/circuits and because the integration of the present particular layers does not produce any unexpected results.

Double Patenting

3. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. **The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.**

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Art Unit: 2815

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b)

5. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application.

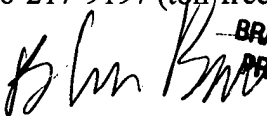
6. Double-patenting conflicts exist between the claims of the present application and claims of the issued patents and co-pending applications associated with the Motorola bulk filing project for the reasons set forth in the double patenting section of the other bulk-filing applications, those reasons being incorporated herein by reference.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to B. William Baumeister whose telephone number is (571) 272-1722. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

 **BRADLEY BAUMEISTER
PRIMARY EXAMINER**

B. William Baumeister
Primary Examiner
Art Unit 2815

June 18, 2004